Low-Noise and Linear FET Amplifiers for Satellite Communications

DAVID A. COWAN, PAUL MERCER, AND ABE B. BELL, MEMBER, IEEE

Abstract—**FET amplifiers with ambient noise figures as low as 4.8 dB at 12 GHz, 35-dB gain, and intercept points as high as +28 dBm have been developed for use in communications satellites. Predicted mean time to failure is in excess of 10^6 h.**

INTRODUCTION

ALTHOUGH microwave FET's have been available for many years they have not become generally accepted for use in systems where ultra-high reliability is required (for example, in communications satellites). Until recently, little information on GaAs FET reliability was available; however, accelerated life testing performed by manufacturers [1], [2], coupled with a reasonable accumulation of long-term device testing, has demonstrated that GaAs FET's can be highly reliable devices with predicted mean time to failure (MTTF) in excess of 10^8 h.

Two 12-GHz FET amplifier types have been developed by Spar Technology Limited, for use in communications satellites. These amplifiers utilize packaged 1-μm gate-length GaAs FET devices which have undergone stringent qualification testing to ensure their long-term reliability. A low-noise and a linear amplifier design have been developed. The low-noise amplifier has an ambient temperature noise figure as low as 4.8 dB with a gain of 35 dB, while for the linear amplifiers, the gain is 35 dB with a third-order intermodulation intercept point as high as +28 dBm. Both amplifiers have good gain flatness, high-temperature stability, and low-group delay. Small size and low weight are of prime importance, and each amplifier operates from a +15-V dc supply, utilizing an integral switching type power converter for minimum power consumption.

FET SPECIFICATION AND QUALIFICATION

The transistor selected for the FET amplifiers was the Nippon NE 24406, a 1-μm gate-length transistor in a hermetic ceramic package. No significant performance penalties are encountered from using a packaged device for at least up to 5-percent operating bandwidths at this frequency. The microwave parameters of the transistors are specified at a frequency of 12 GHz and are based on typical results of characterization in a microstrip test mount. Devices are specifically selected for either low noise figure or high intercept point.

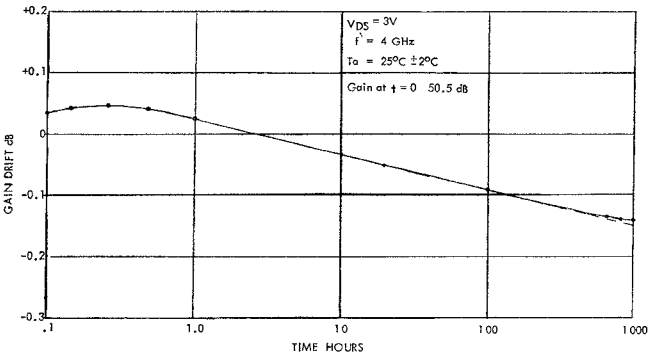

Fig. 1. Gain drift for five-stage amplifier.

Stringent qualification testing of flight devices included power burn-in of all devices for 336 h at elevated temperatures (100 C° ambient) with both dc and RF parameters monitored and checked for drift during this period; ±5-percent ΔI_{DSS} was permitted, and ±0.1-dB ΔMAG (maximum available gain). Short- and medium-term stability were evaluated by selecting five sample devices from each wafer and building them into a five-stage amplifier. The amplifiers were tested over a period of 1000 h and the gain drift with time was monitored; a maximum amplifier gain drift of 0.1 dB per decade of time was permitted. Typical measured value was 0.08 dB/decade. For long-term stability, measurements (Fig. 1) have shown that gain tends to stabilize during the first 1000 h [3]; extrapolating these figures to a spacecraft lifetime of seven years results in a maximum FET gain change of 0.25 dB for a six-stage amplifier (following a 600-h burn-in). Results of accelerated life testing [1], [2] tend to support this small change, together with such life test data as is currently available.

Other qualification tests included a wafer reliability assessment based on accelerated life testing at 295°C on sample devices, Group A testing on all devices and Group B testing on sample devices, using MIL-STD-750 methods. The Group A tests covered measurement of dc parameters such as drain current and gate-reverse current and RF measurement of MAG. The more extensive Group B tests for lot qualification covered mechanical, thermal, and operational life testing for 1000 h at 100°C followed by dc parameter drift measurements. SEM (scanning electron microscope) inspection was carried out on sample devices from each wafer, together with 100-percent X-ray inspection of devices after packaging. All flight devices were checked for short-term ($t < 100$ min) drift characteristics (dc and RF) following the power burn-in.

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D. A. Cowan was with Spar Technology Limited, Saint Anne de Bellevue, Quebec, Canada H9X 3R2. He is now with Continental Microwave Limited, Dustable, England.

P. Mercer was with Spar Technology Limited, Saint Anne de Bellevue, Quebec, Canada H9X 3R2. He is now with MA Electronics Canada Limited, Mississauga, Canada.

A. B. Bell is with Spar Technology Limited, Saint Anne de Bellevue, Quebec, Canada H9X 3R2.

TABLE I
S-PARAMETER MEASUREMENTS—12-GHz FETA

F (GHz)	S11		S12		S21		S22	
11.0	.621	133.2	.033	-54.6	1.337	-38.7	.810	-138.5
11.5	.612	120.7	.032	-67.7	1.28	-52.1	.828	-150.8
11.6	.613	118.7	.032	-70.6	1.27	-54.6	.832	-153.4
11.7	.614	116.2	.031	-73.4	1.26	-57.2	.839	-159.7
11.9	.615	110.9	.036	-79.7	1.241	-63.0	.846	-160.6
12.1	.614	106.9	.029	-86.6	1.218	-69.0	.85	-165.8
12.3	.607	102.5	.029	-98.3	1.197	-75.1	.875	-170.9
12.4	.605	100.1	.027	-104.5	1.178	-78.6	.880	-173.9

Note: NE 24406 transistor—computer corrected transistor *S*-parameters (50-Ω mount).

TABLE II
S-PARAMETER MEASUREMENTS—12-GHz FETA

F (GHz)	S11		S12		S21		S22	
11.0	.380	37.9	.062	-161.8	2.13	-145.7	.783	117.6
11.5	.418	-11.2	.081	164.4	2.55	-179.9	.560	85.5
11.6	.431	-20.0	.083	156.1	2.62	172.3	.500	74.8
11.7	.446	-30.3	.084	147.9	2.66	163.4	.438	61.7
11.9	.466	-47.8	.089	130.9	2.69	145.8	.344	23.7
12.1	.463	-63.2	.090	111.0	2.60	126.7	.354	-27.7
12.3	.446	-74.8	.088	88.8	2.39	107.0	.475	-69.9
12.4	.435	-78.6	.084	77.6	2.25	97.9	.540	-85.0

Note: NE 24406 transistors with single-stage input and output matching transformers—computer corrected *S*-parameters (partially matched mount).

DEVICE CHARACTERIZATION

If computer-aided design techniques are to be used for amplifier modules it is essential to perform accurate device *S*-parameter measurements. At 12 GHz the parameters depend to a large extent on the test mount used for characterization (for example, the S_{12} value for the transistor may be considerably modified by feedback within the test mount); the test-mount configuration should, therefore, resemble closely the mounting configuration to be used in amplifier modules. The test mount used comprised microstrip transmission lines at input and output to the transistor with printed bias networks and beam-lead capacitors for dc isolation. The width of the test-mount cavity was less than $\lambda/2$ at the maximum frequency of operation to eliminate waveguide feedback modes. The mount was characterized on an automatic network analyzer before mounting the transistors, and an equivalent circuit was derived; this was used in the correction of transistor *S*-parameters to a convenient design reference plane, in conjunction with a network analysis program used on a time sharing computer.

Initial characterization was carried out using 50-Ω characteristic impedance input and output lines; for more accurate measurements a partially matched mount, comprising single stage input and output matching transformers, was used. Typical corrected *S*-parameter measurements are given in Table I and Table II.

Optimum source impedance for low-noise performance was determined empirically and found to be close to a conjugate input match to the transistor. The optimum load impedance for intermodulation products was also determined empirically by tuning for maximum saturated power output. Typical bias conditions were $V_{DS} = 4.5$ V, $I_{DS} = 10$ mA, for low-noise devices, and $V_{DS} = 5.0$ V, $I_{DS} = 25$ mA, for low intermodulation product devices. Typical MAG was found to be in excess of 8 dB for low-noise devices and 9 dB for other devices.

TABLE III
LOW-NOISE AMPLIFIER—GAIN BUDGET

COMPONENT	GAIN (dB)	LOSS (dB)
Input & Output Connections including Stress Relief		-0.7
Isolators Qty 4		-1.6
PIN Attenuator		-4.0
Low-Noise Two-Stage Amplifier Module	+13.0	
High-Gain Two-Stage Amplifier Modules Qty 2	+30.0	
Net Gain	+36.7 dB	

AMPLIFIER DESIGN

A single-ended design approach, with isolator coupling, was used. Advantages of the single-ended approach include lower cost (a significant figure in the case of flight-qualified devices), higher reliability due to a lower component count, and lower power consumption.

A modular design approach has been developed for MIC (microwave integrated circuit) FET amplifiers and offers many advantages when compared with a single integrated unit. Individual modules are tuned in test mounts prior to "drop-in" integration into the amplifier assembly, enabling optimum performance to be achieved from each module and reducing the time required for tuning. Repairs can be quickly and conveniently carried out by simply replacing modules, and problem areas which arise on integration can be readily identified. Module types used in the amplifiers include low-noise, high-gain, and linear two-stage amplifiers, isolators and p-i-n attenuators.

Each of the two amplifier types contains three two-stage amplifier modules (six FET's) with isolator modules between them and at the input and output ports to the amplifiers. A p-i-n attenuator module, located either before or after the second amplifier module (depending on the amplifier type), is used to achieve compensation of the amplifier gain change with temperature. The p-i-n attenuator can provide a dynamic range of several decibels with a very small gain slope variation. The position of the attenuator modules was chosen to have minimum effect on noise figure of the low-noise amplifier and on intermodulation products in the linear amplifier.

The schematic for the low-noise amplifier is shown in Fig. 2. Biasing and matching transistors for low-noise or low-intermodulation products rather than maximum gain, together with circuit losses (including isolators), and p-i-n attenuator losses, results in the need for six stages to achieve 35-dB overall gain. The design gain margin is then 2 dB, based on the gain budget shown in Table III.

The three two-stage amplifier module types were designed using typical measured *S*-parameter data, with the aid of a computer optimization program. (There is a brief descrip-

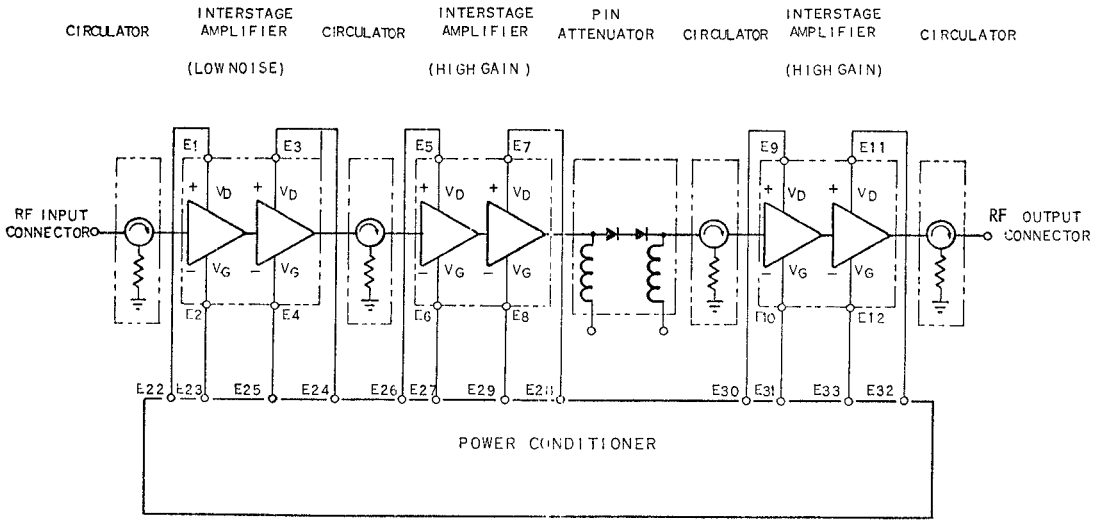

Fig. 2. Low-noise amplifier schematic.

tion of the program given in the Appendix.) Matching is accomplished using distributed elements only, except that ferrite beads are required on the dc bias filtercons to provide resistive loading at low frequencies and thus ensure stability; a printed low-pass filter structure ensures that the bias network is purely reactive at 12 GHz. MOS beam lead capacitors, which have low-reflection coefficients when mounted in series in a 50-Ω transmission line, are used to achieve dc isolation.

The MIC isolator modules are three-port circulators printed on yttrium garnet substrates, with a stubmatched 50-Ω chip resistor to terminate the third port. The design achieves low output to input coupling by suppressing radiation from the circulator disc. A minimum isolation of 26 dB with less than a 0.3-dB insertion loss is achieved.

Each p-i-n attenuator module comprises two series-mounted beam lead diodes (a "fail safe" configuration, since p-i-n diodes normally fail short circuit) spaced approximately one-quarter wavelength apart to achieve low VSWR. The drive circuit for the diodes consists of a thermistor-controlled current source whose resistor elements are computer optimized to achieve the best temperature compensation curve fit.

Power Converter Design

The common-source FET mounting configuration used in the amplifier requires both positive and negative voltage bias rails for each transistor. High stability in both the short and long term is important for good amplifier gain stability. High efficiency is a prime requirement due to the maximum available power of 1.5 W for each amplifier.

The power converter design employs a pulsewidth modulated buck-type switching regulator, resulting in efficient conversion of the available +15-V supply voltage to a +5.7-V drain supply and −5.0-V gate supply. A slow start-up circuit is employed to prevent voltage overshoots; this is desirable for reliable FET operation since voltage spikes can cause damage. High regulation is obtained by using high-stability components and a feedback loop with high gain. Filter networks at input and output to the converter result in low ripple on the bias rails and prevent current overshoots.

Biasing of individual transistors is achieved through series resistors in the positive-drain supply, and through two resistors comprising a voltage divider network to each gate in the negative supply. The p-i-n attenuator drive circuit derives its power from the +5.7-V rail. The power converter efficiency is in excess of 75 percent over the full operating temperature range.

Mechanical Design and Layout

Amplifier and p-i-n attenuator modules are constructed with 0.025-in thick 99.5-percent alumina substrates, soldered to nickel-plated Kovar carriers; and the isolator modules are constructed with 0.025-in garnet substrates soldered to a nickel-plated nickel–iron alloy carrier. In both cases the thermal-expansion coefficient of substrate and carrier are closely matched to reduce stresses during temperature cycling. Stress-relieved bonds are used to interconnect modules, both for the RF line and the ground plane. The amplifier housing is machined from aluminum and is nickel plated.

The amplifier layout is determined primarily by RF considerations. All modules are designed to be in cut-off waveguide sections when the amplifier cover is on, resulting in low reverse feedback and high stability. The power converter is completely isolated from the RF circuits, with the bias supplies to transistors being fed through filtercons mounted on the Kovar carrier. A photograph of the linear amplifier is shown in Fig. 3.

Overall size of the amplifier is approximately three and one-half inches square by one inch deep, and the weight is 0.84 lb. Vibration testing showed that all stress margins were adequate.

Amplifier Reliability

All components and materials used in the amplifiers are subjected to the usual screening requirements for use in high

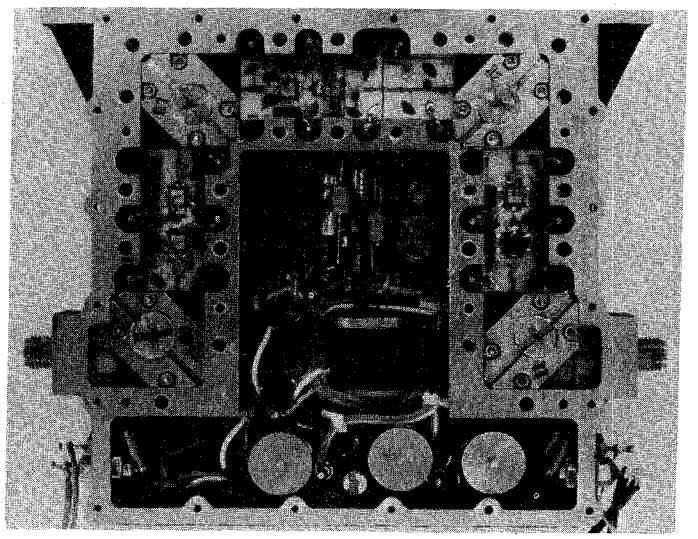

Fig. 3. Linear FET amplifier.

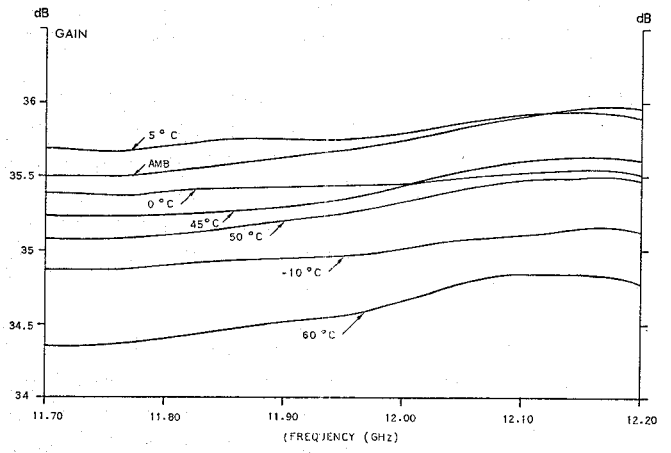

Fig. 4. Gain—linear FET amplifier.

reliability applications, and rigorous inspection is carried out by quality control personnel at all stages of manufacture and test.

A computation of MTTF and a worst-case analysis were carried out. For the complete amplifier, including power converter, a failure rate of 876 FITS (failures in 10^9 h) is predicted; this includes a contribution of 362 FITS for the power converter, and assumes a failure rate of 64 FITS for each transistor (maximum channel temperature 82°C). Worst-case analysis for a seven-year operation shows the most significant performance change to be due to ageing of components in the p-i-n attenuator drive circuit. Summing the effects of power converter-bias network, FET, and p-i-n attenuator ageing, results in a worst-gain stability of +0.61 dB, −1.09 dB, $T_{amb} = 5°C$ as shown in Table IV. The worst-case change of the noise figure is 0.4 dB, and of the third-order intercept point is 0.21 dB. These figures are sufficiently small to ensure that specification will be met over the full spacecraft lifetime.

Such data as have so far been published on GaAs FET sensitivity to radiation and particle bombardment [4], [5], suggest that these devices are relatively immune. It is estimated that the ionizing radiation dose absorbed by the devices will be limited to 10^5 rad by the spacecraft structure and amplifier and receiver enclosures, and that particle fluence will not exceed $2 \times 10^{13}/cm^2$. These figures are well below the thresholds at which damage to FET's has been recorded.

TABLE IV
WORST-CASE GAIN CHANGE OVER SEVEN-YEAR LIFE

T °C	5	25	45
Δ L_{PIN} dB	+.76 -.35	+.35 -.20	+.14 -.07
Δ G_{FET} dB	+.00 -.24	+.00 -.24	+.00 -.24
Δ G_{BIAS} dB	+.26 -.09	+.26 -.09	+.26 -.09
Δ G_{TOT} dB	+.61 -1.09	+.46 -.68	+.33 -.47

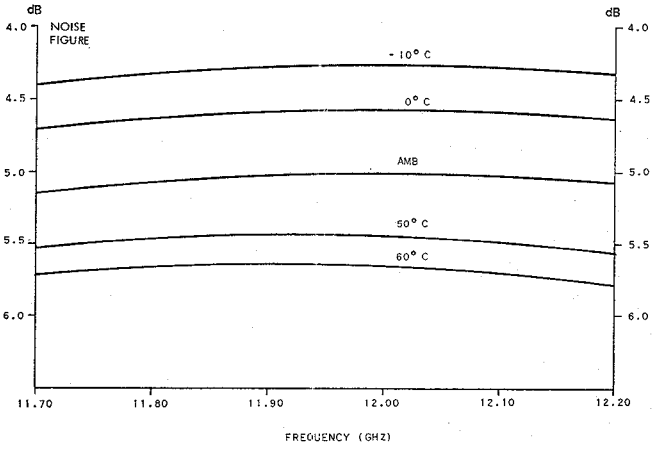

Fig. 5. Noise figure—low-noise amplifier.

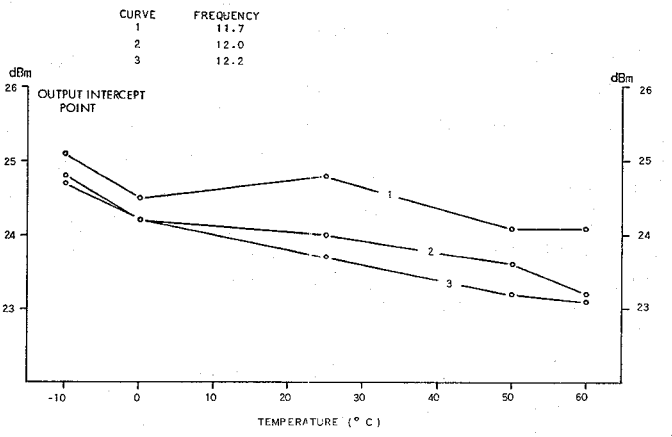

Fig. 6. Intercept point—linear amplifier (10-MHz frequency separation).

MEASURED PERFORMANCE

All modules were tuned and tested individually prior to integration and found to meet or exceed their design goals.

TABLE V
SPECIFICATION AND PERFORMANCE SUMMARY

Parameter	Specification		Measured Performance (Worst Case Over Spec. Temperature Range)	
Operating Frequency Range 11.7 to 12.2 GHz Unless stated otherwise	Parameter Specification	Applicable Temperature Range (°C)	Low Noise Amplifier	Linear Amplifier
Midband Gain	35 dB + 2, -0 dB	25	38.65 dB	35.75 dB
Gain Variation over Frequency Band	1.0 dB peak-to-peak maximum	0–50	0.40 dB	0.50 dB
Gain Stability	1.25 dB peak-to-peak maximum	5–45	0.80 dB	0.50 dB
Gain Slope	.004 dB/MHz maximum	0–50	0.003 dB/MHz	0.0032 dB/MHz
Noise Figure	7 dB maximum (low noise) 10 dB maximum (linear)	0–50	5.6 dB	9.5 dB
Port VSWR	1.25:1 maximum	0–50	1.11:1 Input Port 1.10:1 Output Port	1.20:1 Both Ports
Group Delay Variation	0.5 ns maximum	0–50	0.4 ns	0.5 ns
Linearity	Third-Order Intercept Point +17 dBm minimum (low noise) +23 dBm minimum (linear)	0–50	+20.3 dBm	+23.2 dBm
Spurious Outputs	-75 dBm maximum	0–50	None detectable	None detectable
Power Consumption	1.5W maximum	0–50	1.09W	1.27W
Voltage Variation	15V±5%	0–50	No measureable effect on Gain Frequency Response, Noise Figure, Linearity.	
Weight	0.75 lb maximum	-	0.84 lb	0.84 lb

Following integration into the amplifier housing, a little additional tuning was required to achieve the overall amplifier specifications. This is due primarily to the small mismatches introduced by the flexible module interconnections and due to evanescent radiation modes which tend to degrade performance by mutual coupling between modules.

The significant electrical parameters were recorded over several temperature cycles with the extremes $\pm 10°C$ in excess of the 0–50°C design temperature range. A summary of the test results for the first development models of both amplifier types is given in Table V. Using better FET's subsequently obtained from the supplier, a 0.4-dB noise-figure improvement and a 4-dB intercept-point improvement, were achieved. Design specification values are given in the table, and it can be seen that all important requirements are met.

Referring to Table V, the midband gains for the low-noise and linear amplifiers are 38.65 and 35.78 dB, respectively, with 0.4- and 0.5-dB gain flatness over the 500-MHz operating frequency band. The higher gain in the low-noise unit is due to higher module gains than the design target. The worst-case gain slope is 0.003 dB/MHz. The high stability of the gain slope with temperature is demonstrated in the Fig. 4 plot of the linear amplifier gain and is a result of the design strategy of employing a constant bias on the FET's and a well-matched p-i-n diode attenuator for temperature compensation. Within the optimized 5–45°C temperature range, gain variations of 0.8 and 0.5 dB for the low-noise and linear amplifiers were measured.

The noise figure characteristic of the low-noise amplifier is given in Fig. 5. A worst-case value of 5.6 dB was measured at 50°C. This performance was achieved by the selection of front-end FET's which have a 3.9-dB noise figure at 25°C, and by minimizing the loss of the input isolator.

The group-delay variation was very small. At the temperature extremes, the variation was 0.4 and 0.5 ns over the 500-MHz band, for the low-noise and linear amplifiers, respectively.

The third-order intercept point of the linear amplifier is shown for several operating frequencies in Fig. 6. The worst-case intercept point is 23.2 dBm. No linearity variation was observed with changing carrier separation (0.5 to 50 MHz Δf was tested) indicating effective decoupling of the converter supply from the RF circuitry.

The amplifier power consumptions are well below the 1.5-W maximum, with a power consumption variation of less than 5 percent over the operating temperature range. This reflects the low-current requirement of the p-i-n attenuator, the use of constant bias on the FET's, and the relatively constant converter efficiency over the temperature range.

Radiated susceptibility testing was carried out on the low-noise amplifier and showed that the unit was essentially connector limited. With a 1-V/m field strength, an output power of -67-dBm maximum was observed with incidence around the input port.

CONCLUSION

Design and measured data have been given for a low-noise and a highly linear 12-GHz FET amplifier. It is felt that these amplifiers represent the state-of-the-art for high-reliability amplifiers in this frequency range, particularly for the gain slope and gain stability, and noise figure and group delay characteristics. Reliability predictions indicate that the probability of survival for such amplifiers over communications satellite lifetime, is at least as high as alternative types of amplifiers that are currently available, and it is likely that they will find increasing application in high-reliability systems.

APPENDIX

The computer optimization program used is an in-house program called COSMIC-K, which stands for computer optimization of simple microwave integrated circuits, kronos time-sharing. Although written for microwave circuits, it accommodates all lumped or distributed circuit elements that can be represented by a complex 2×2 matrix, including *RLC* circuits, microstrip lines, and *S*-parameters.

The program consists of a network analysis section and a minimum-seeking algorithm, plus the necessary connective software. The minimum-seeking algorithm follows the literature [6]. In order to try to guarantee finding a global minimum and not a local minimum, a limited grid search is used.

To apply the optimization capability, the user indicates which of the circuit elements are to be varied and over what permissible limits. He also inputs weights and limits on up to four circuit characteristics to be optimized. The program then finds the element values at which the circuit performance comes closest to the desired characteristics.

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A 12-GHz Low-Cost Earth Terminal for Direct TV Reception from Broadcast Satellites

RENE J. DOUVILLE, MEMBER, IEEE

Abstract—**A low-cost 12-GHz receiver for TV reception from high-power broadcast satellites is described. System designs using 0.6- and 1.2-m parabolic dishes with high-efficiency Cassegrain and prime-focus feed configurations have been studied. The front end consists of an MIC image-enhanced mixer, 1.2-GHz low-noise amplifier, and a Gunn diode LO. The signal is then fed to an indoor unit which has been designed using both surface acoustic wave (SAW) and lumped element 70-MHz bandpass filters and demodulators. Audio and video receiver outputs are fed directly to the baseband circuitry of a standard receiver.**

I. INTRODUCTION

HERMES communications technology satellite operating at 12 GHz and with an EIRP of 59 dBW ushered in the era of the high-power broadcast satellite [1]. In early 1978 Japan will be launching a similar satellite with an EIRP of up to 57 dBW [2]. The Nordic countries (Nordsat) [3] and West Germany [2] are seriously considering domestic high-power (60–67-dBW) broadcast satellite systems. Such systems permit the use of small TV receive-only terminals with values of G/T as low as 5 dB/K. This paper describes the development of such a terminal, discusses various alternatives which were considered, and comments on some of the advantages and disadvantages of each. The overall goal was to realize component designs which would lend themselves readily to low-cost medium-to-large-volume production.

II. SYSTEM CONFIGURATION

Fig. 1 illustrates the system configuration which was adopted. Table I lists some of the target system parameters. Note that the design bandwidth of the terminal under construction was 85 MHz (although only 30 MHz per channel is actually required). However, some effort was made to anticipate future requirements for operation over the full 500-MHz allocated band. A double conversion approach was selected over single conversion. AFC on the second LO permits the use of super high frequency (SHF) LO's with relaxed long-term and temperature stability requirements. Also, future requirements for multichannel reception can be met by switching the second LO.

The single conversion approach would not only require the first LO to be remotely tunable to pre-set frequencies over the 500-MHz satellite band, but it would also be

TABLE I
TARGET SYSTEM PARAMETERS (1.2-m DISH)

Frequencies - Signal	12.038 - 12.123 GHz[1]
- SHF LO	10.8805 ± 0.005 GHz
- 1st IF	1.200 GHz
- UHF LO	1.130 ± .005 GHz
- 2nd IF	70.0 ± 0.2 MHz
Polarization	Linear
G_a/T_s	11.5 dB/°K (beam centre)
Outdoor Unit Gain	> 26.0 dB
UHF Cable (RG213U)	15m (<6 dB loss)
Indoor Unit Noise Figure	< 12 dB
Noise Bandwidth	22 MHz
Differential Phase	< 4°
Differential Gain	< 15%
Video Signal-to-Noise Ratio[2]	> 39 dB at threshold
Audio Signal-to-Noise Ratio[3]	> 45 dB at threshold
Audio Subcarrier Frequency	5.14 MHz
Outdoor Unit - Temperature Range	- 40°C to + 50°C
- Humidity	5% to 100%

[1] Actual band used is 12.0655-12.0955.
[2] Video peak to peak weighted (excluding sync. tip) to rms weighted noise.
[3] Audio rms TT/N weighted.

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The author is with the Communications Research Centre, P.O. Box 11490, Station "H," Ottawa, Ont., Canada.